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Claims

[c1] 1. A method of manufacturing a semiconductor device comprising the steps of:
forming a first conductive film on a gate insulating film formed in first and second areas of a semiconductor substrate;
selectively removing the first conductive film to form a gate electrode of a first MIS transistor in the first area and a conductive pattern covering a whole surface of the second area;
forming side wall spacer insulating films made of a first insulating film on side walls of the gate electrode of the first MIS transistor;
by using the gate electrode of the first MIS transistor as a mask, introducing impurities into the first area to form source/drain diffusion regions of the first MIS transistor;
forming a second insulating film over the semiconductor substrate including the first and second areas;
selectively removing the second insulting film and the first conductive film to form a lamination pattern of a gate electrode of a second MIS transistor in the second area;
by using the lamination pattern as a mask, introducing

impurities into the second area to form source/drain diffusion regions of the second MIS transistor;
forming side wall spacer insulating films made of a third insulating film on side walls of the lamination pattern; and
forming a second conductive film connecting at least one of the source/drain diffusion regions in the second area.

[c2] 2. A method of manufacturing a semiconductor device according to claim 1, further comprising a step of introducing impurities into the first area to form the source/drain diffusion regions of the first MIS transistor and also into the gate electrode of the first MIS transistor.

[c3] 3. A method of manufacturing a semiconductor device according to claim 2, further comprising a step of selectively forming a metal silicide film on the source/drain regions and the gate electrode of the first MIS transistor, after said step of introducing impurities into the first area.

[c4] 4. A method of manufacturing a semiconductor device comprising the steps of:
(a) forming a first conductive film on a gate insulating film formed in first and second areas of a semiconductor substrate;
(b) selectively removing the first conductive film to form

a gate electrode of a first MIS transistor in the first area and a conductive pattern covering a whole surface of the second area;

(c) forming side wall spacer insulating films made of a first insulating film on side walls of the gate electrode of the first MIS transistor;

(d) by using the gate electrode of the first MIS transistor as a mask, introducing impurities into the first area to form source/drain diffusion regions of the first MIS transistor and also into the gate electrode and the conductive pattern;

(e) selectively forming a metal silicide film on the source/drain regions and the gate electrode of the first MIS transistor and on the conductive pattern;

(f) forming a second insulating film over the semiconductor substrate including the first and second areas;

(g) selectively removing the second insulting film and the first conductive film to form a lamination pattern of a gate electrode of a second MIS transistor in the second area;

(h) by using the lamination pattern as a mask, introducing impurities into the second area to form source/drain diffusion regions of the second MIS transistor;

(i) forming side wall spacer insulating films made of a third insulating film on side walls of the lamination pattern; and

(j) forming a second conductive film connected to at least one of the source/drain diffusion regions in the second area.

[c5] 5. A method of manufacturing a semiconductor device according to claim 4, wherein the first insulating film is a silicon oxide film and the third insulating film is a silicon nitride film.

[c6] 6. A method of manufacturing a semiconductor device according to claim 4, wherein said step (b) forms also a gate electrode of a third MIS transistor in the first area, said step (d) introduces impurities into the first area to form the source/drain regions of the first MIS transistor and also into the gate electrode of the first MIS transistor, by covering an area containing the gate electrode of the third MIS transistor with a mask, and the method further comprises a step of:
(k) introducing impurities into the first area while covering the first MIS transistor with a mask, to form source/drain regions on both sides of the gate electrode of the third MIS transistor and also into the gate electrode of the third MIS transistor.

[c7] 7. A method of manufacturing a semiconductor device, comprising the steps of:
forming a plurality of word lines in a memory cell area of

a semiconductor substrate, the word line having a lamination structure of a first conductive film and a first insulating film;
by using the lamination structure as a mask, introducing impurities into the semiconductor substrate to form source/drain regions;
forming first side wall spacer insulating films on side walls of the lamination structure, the first side wall spacer insulating film having substantially a same etching characteristic as the first insulating film;
forming a second insulating film on the memory cell area, the second insulating film having an etching characteristic different from the first insulating film;
selectively etching the second insulating film on one of the source/drain regions on both sides of the word line in the memory cell area to form a first contact hole defined by the first side wall spacer insulating film;
filling an inside of the first contact hole with a second conductive film;
forming a third conductive film and a third insulating film on the second insulating film to cover the second conductive film filled in the first contact hole, the third insulating film having an etching characteristic different from the second insulating film, and patterning the third insulating film and the third conductive film to form a bit line electrically connected to said one of the source/

drain regions via the second conductive film;
forming second side wall spacer insulating films on side walls of the bit line made of the third insulating film and the third conductive film, the second side wall insulating film having an etching characteristic different from the second insulating film;
forming a fourth insulating film on the second insulating film, to cover the bit line, the fourth insulating film having substantially a same etching characteristic as the second insulating film;
selectively and sequentially etching the fourth and second insulating films above the other of the source/drain regions opposing to said one source/drain across said word line in the memory cell area, to form a second contact hole defined by the second and first side wall spacer insulating films; and
forming a storage electrode electrically connected to the other of the source/drain regions via the second contact hole.

[c8] 8. A method of manufacturing a semiconductor device, comprising the steps of:
(a) forming element isolation insulating films in first and second areas of a semiconductor substrate to define active regions;
(b) depositing a first conductive film on a whole surface

of the semiconductor substrate;

(c) forming a first mask member on the first conductive film, the first mask member covering the first area and exposing the second area;

(d) by using the first mask member as a mask, etching the first conductive film to leave the first conductive film extending in the first area;

(e) by using the first mask member or the first conductive film as a mask, introducing impurities into the semiconductor substrate in the second area;

(f) depositing a second conductive film over a whole surface of the semiconductor substrate;

(g) forming a second mask member on the second conductive film, the second mask member having a pattern of gate electrodes to be formed in the second area;

(h) by using the second mask member as a mask, etching the second conductive film to form a plurality of second gate electrodes in the second area; and

(i) patterning the first conductive film in the first area to form a plurality of first gate electrodes.

[c9] 9. A method of manufacturing a semiconductor device according to claim 8, further comprising between said step (h) and said step (i) a step of:

(j) by using as a mask the first conductive film in the first area and the plurality of gate electrodes in the second

area, introducing impurities into the second area to form second source/drain regions.

[c10] 10. A method of manufacturing a semiconductor device according to claim 8, wherein said step (b) forms the first conductive film and a first insulating film on the first conductive film, and said steps (d) and (i) etches the first insulating film and the first conductive film in a same pattern.

[c11] 11. A method of manufacturing a semiconductor device according to claim 8, wherein said step (f) forming a second insulating film on the second conductive film and said step (h) etches the second insulating film and the second conductive film in a same pattern.

[c12] 12. A method of manufacturing a semiconductor device according to claim 9, further comprising a step of:
(k) introducing impurities into the first area to lower respective resistances of the first gate electrode and semiconductor substrate surface layers on both sides of the first gate electrode.

[c13] 13. A method of manufacturing a semiconductor device according to claim 12, wherein said step (h) introduces n- and p-type impurities by using different mask members.

[c14] 14. A method of manufacturing a semiconductor device according to claim 8, wherein the second conductive film is a lamination of a doped silicon layer and a silicide layer.

[c15] 15. A method of manufacturing a semiconductor device according to claim 12, wherein the first conductive film is made of silicon, and the method further comprises before said step (f) a step of:
(l) forming a thermal oxide film on surfaces of the second area and the first conductive film.

[c16] 16. A method of manufacturing a semiconductor device according to claim 15, wherein said step (k) comprises the steps of:
(k-1) implanting first ions into the first area;
(k-2) forming side spacers on side walls of the first gate electrode and forming a third insulating film covering the second area; and
(k-3) implanting second ions into the first area formed with the side spacers to form first source/drain regions having a high impurity concentration and the first gate electrode having a low resistance.

[c17] 17. A method of manufacturing a semiconductor device according to claim 16, further comprising a step of:

(m) selectively forming a silicide film on the first source/drain regions and first gate electrode in the first area.

[c18] 18. A method of manufacturing a semiconductor device according to claim 17, further comprising a step of:
(n) forming a lamination of an etching resistant insulating film and a first interlayer insulating film over a whole surface of the semiconductor substrate, after said step (m).

[c19] 19. A method of manufacturing a semiconductor device according to claim 17, further comprising the steps of:
(o) etching the first interlayer insulating film on the second source/drain regions in the second area, by using the etching resistant insulating film as an etching stopper, after said step (m);
(p) etching the exposed etching resistant insulating film to form a first contact hole reaching the second source/drain region; and
(q) forming a conductive plug in the first contact hole.

[c20] 20. A method of manufacturing a semiconductor device according to claim 19, further comprising the steps of:
(r) forming a second interlayer insulating film on the first interlayer insulating film, the second interlayer insulating film covering the conductive plug;
(s) by using as an etching mask the etching resistant in-

sulating film or the conductive plug, etching the second and first interlayer insulating films to form a second contact hole; and

(t) forming a wiring layer embedding the second contact hole.

[c21] 21. A method of manufacturing a semiconductor device according to claim 19, wherein the semiconductor substrate has an intermediate area between the first and second areas, said step (h) forms a contact portion for a word line on the element isolation insulating film in the intermediate area, said step (k-2) forms a third insulating film at least partially exposing the contact portion of the word line in the intermediate area, said steps (o) and (p) form a third contact hole exposing at least partially the contact portion of the word line in the intermediate area, and said step (q) forms also the conductive plug embedding the third contact hole.

[c22] 22. A semiconductor device, comprising:

a semiconductor substrate including first and second areas;

a plurality of first conductive patterns formed in the first area;

a plurality of second conductive patterns formed in the second area, said second conductive pattern having a structure different from said first conductive pattern;

first, second, third and fourth insulating films formed on said second conductive pattern; and
said third and fourth insulating films formed on the first conductive pattern.

[c23] 23. A semiconductor device according to claim 22, further comprising side spacers formed on side walls of said first conductive pattern, said side spacer having a same composition as said second insulating film.

[c24] 24. A semiconductor device according to claim 23, further comprising:
first source/drain regions formed in a surface layer of said semiconductor substrate on both sides of said first conductive pattern, said first source/drain regions not formed with a silicide layer; and
second source-drain regions formed in a surface layer of said semiconductor substrate on both sides of said second conductive pattern, said second source/drain regions formed with a silicide layer.

[c25] 25. A method of manufacturing a semiconductor device, comprising the steps of:
(a) forming element isolation insulating films in first and second areas of a semiconductor substrate to define active regions;
(b) depositing a lamination structure of a first conductive

film and a first insulating film on a whole surface of the semiconductor substrate;

(c) forming a first mask member on the lamination structure, the first mask member having a pattern of a wiring forming area in the second area;

(d) by using the first mask member as a mask, etching the first insulating film of the lamination structure to leave the first insulating film only in the wiring forming area in the second area;

(e) removing the first mask member;

(f) forming a second mask member on the first conductive film in the first area, the second mask member having a pattern of a wiring forming area; and

(g) etching the first conductive film by using as a mask the second mask member and the left first insulating film.

[c26] 26. A method of manufacturing a semiconductor device according to claim 25, wherein said step (b) comprises the steps of:

(b-1) forming a semiconductor film;

(b-2) selectively doping impurities into the semiconductor film in the second area; and

(b-3) forming the first insulating film on the semiconductor film selectively doped with the impurities.

[c27] 27. A method of manufacturing a semiconductor device according to claim 26, further comprising the steps of:
(h) implanting first ions into the first area;
(i) forming side spacers on side walls of the first gate electrode and forming a second insulating film covering the second area; and
(j) implanting second ions into the first area formed with the side spacers to form first source/drain regions of a high impurity concentration and the first gate electrode having a low resistance.

[c28] 28. A semiconductor device, comprising:
a semiconductor substrate having first and second areas and an intermediate area;
a first gate electrode structure formed in the first area, said first gate electrode structure having a plurality of first conductive patterns;
a second gate electrode structure formed in the second area, said second gate electrode structure having a lamination structure of a plurality of second conductive patterns having a same structure as said first conductive patterns, and a first insulating film having a same pattern and formed on said second conductive pattern;
a third gate electrode structure formed of a lamination of a third conductive pattern formed in the intermediate area, said third conductive pattern having a same struc-

ture as said first conductive pattern, and a second insulating film formed on a partial surface of said third conductive pattern and having a same structure as said first insulating film; and

an upper insulating film formed on surfaces of said first, second and third gate electrode structures.

[c29] 29. A semiconductor device comprising:

a semiconductor substrate;

a memory cell area and a logic area defined in said semiconductor substrate;

word lines formed in said memory cell area, said word line including a gate electrode;

gate electrodes of complementary transistors formed in said logic area;

first insulating layers made from a same layer formed on an upper surface of said word line in said memory cell area and on side walls of said gate electrode in said logic area; and

second insulating layers made from a same layer covering side walls of said word line in said memory cell area and covering said gate electrode in said logic area.

[c30] 30. The semiconductor device recited in claim 29, further comprising:

side wall spacers formed on side walls of but not on an upper surface of said word line in said memory cell area;

and

side wall spacers formed on side walls of but not on an upper surface of said gate electrodes in said logic area.

[c31] 31. A semiconductor device comprising:

a semiconductor substrate;

a memory cell area and a logic area defined in said semiconductor substrate;

word lines formed in said memory area, said word line including a gate electrode;

gate electrodes of complementary transistors formed in said logic area;

a first insulating layer formed on said word line in said memory area, said first insulating layer having substantially a same pattern as said word line;

a second insulating layer formed over side walls of said gate electrode in said logic area; and

a third insulating layer formed over an upper surface of said gate electrode in said logic area; and

fourth insulating layers covering side walls of said word line and said gate electrode in said logic area,

wherein a thickness of said first insulating layer is equal to a sum of thicknesses of said second and third insulating layers.

[c32] 32. The semiconductor device recited in claim 31, further comprising:

side wall spacers formed on side walls of but not on an upper surface of said word line in said memory cell area; and

side wall spacers formed on side walls of but not on an upper surface of said gate electrodes in said logic area.